UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,263	10/21/2003	Dominik J. Schmidt	6057-60502	4606

35690 7590 11/14/2007

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
FRANKLIN, RICHARD B	

ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
11/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,263	SCHMIDT, DOMINIK J.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 10 are pending.

Reopening of Prosecution After Appeal Brief

2. In view of the Appeal Brief filed on 02 August 2007, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Response to Arguments

3. Applicant's arguments, see pages 1 – 23, filed 02 August 2007, with respect to the rejection(s) of claim(s) 1 – 10 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of US Patent No. 6,925,510, US Patent No. 5,931,933, and US Patent No. 5,440,244.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 6 – 8 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,925,510 (hereinafter Yu).

As per claim 1, Yu teaches an interface circuit conforming to multiple bus standards (Figure 3 Item 220) comprising a fist interface circuit conforming to a first bus standard (Figure 3 Item 224); a second interface circuit conforming to a second bus standard (Figure 3 Item 222); and a common set of pins (Figure 3 [connection between peripheral device 220 and bus 230]) coupled to the first and second interface circuit and

a host computer bus (Figure 3 Item 230), the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard (Col 5 Lines 17 – 25).

As per claim 6, Yu also teaches wherein the system further comprises an internal bus coupled to the first and second interface circuit (Figure 3 "Internal Bus").

As per claim 7, Yu also teaches wherein the first interface circuit is configured to format signals on the internal bus to signals compliant with the first bus standard (Col 5 Lines 5 – 7).

As per claim 8, Yu teaches an interface circuit (Figure 3 Item 220) comprising a fist interface circuit conforming to a first bus standard (Figure 3 Item 224); a second interface circuit conforming to a second bus standard (Figure 3 Item 222); and a common set of pins (Figure 3 [connection between peripheral device 220 and bus 230]) coupled to the first and second interface circuit and a host computer bus (Figure 3 Item 230), the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard (Col 5 Lines 17 – 25); and an internal bus coupled to the first and second interface circuit (Figure 3 "Internal Bus"), wherein the first interface circuit is configured to format signals on the internal bus to signals compliant with the first bus standard (Col

5 Lines 5 – 7) and the second interface circuit is configured to format signals on the internal bus to signals compliant with the second bus standard (Col 5 Lines 5 – 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 – 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,925,510 (hereinafter Yu) in view of US Patent No. 5,931,933 (hereinafter Billheimer).

As per claims 2 – 4, Yu teaches the system as described per claim 1 (see rejection of claim 1 above).

Yu does not teach wherein the first and second standards are PCI and PCMCIA.

However, Billheimer teaches a bus format conversion circuit comprising a PCMCIA (Billheimer; Figure 1 Item 126) and a PCI (Billheimer; Figure 1 Item 128) translation circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Yu to include the two standards because doing so allows for a single chip to be used in any of several protocols (Billheimer; Col 1 Lines 52 – 53).

6. Claims 5, and 9 – 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,925,510 (hereinafter Yu) in view of US Patent No. 5,440,244 (hereinafter Richter).

As per claim 5, Yu teaches the system as described per claim 1 (see rejection of claim 1 above).

Yu does not teach a multi-voltage input output buffer coupled to each pin.

However, Richter teaches a bi-directional multi-voltage buffer used in an interface (Richter; Col 5 Lines 45 – 65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Yu to include the multi-voltage buffer because doing so allows for avoiding damage to the system in the event of a power mismatch (Richter; Col 6 Lines 32 – 34).

As per claim 9, Yu teaches the system as described per claim 1 (see rejection of claim 1 above).

Yu does not teach a first power supply to supply voltage swings in accordance with the first bus standard.

However, a first power supply to supply voltage swings in accordance with the first bus standard (Richter; Figure 14 "PSV1", Col 24 Lines 22 – 25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Yu to include the power

supply because doing so allows for multiple voltages to be utilized in the system (Richter; Col 23 Lines 49 – 52).

As per claim 10, Yu teaches an interface circuit (Figure 3 Item 220) comprising a fist interface circuit conforming to a first bus standard (Figure 3 Item 224); a second interface circuit conforming to a second bus standard (Figure 3 Item 222); and a common set of pins (Figure 3 [connection between peripheral device 220 and bus 230]) coupled to the first and second interface circuit and a host computer bus (Figure 3 Item 230), the common set of pins being user selectable to communicate with the host computer bus in accordance with either the first bus standard or the second bus standard (Col 5 Lines 17 – 25).

Yu does not teach a first power supply to supply voltage swings in accordance with the first bus standard; and a second power supply to supply voltage swings in accordance with the second bus standard.

However, a first power supply to supply voltage swings in accordance with the first bus standard (Richter; Figure 14 "PSV1", Col 24 Lines 22 – 25); and a second power supply to supply voltage swings in accordance with the second bus standard (Richter; Figure 14 "PSV2", Col 24 Lines 22 – 25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Yu to include the power supply because doing so allows for multiple voltages to be utilized in the system (Richter; Col 23 Lines 49 – 52).

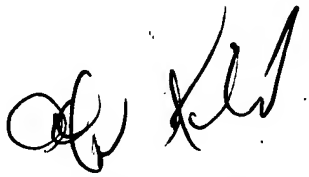
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Franklin
Patent Examiner
Art Unit 2181



ALFORD KINDRED
SUPERVISORY PATENT EXAMINER